==========

S&D4RCES: International workshop on Security and Dependability for Resource Constrained Embedded Systems (Secure and dependable RCES by design)
in conjunction with SAFECOMP 2010 conference (http://www.safecomp.org/)
Vienna, Austria, 14 September 2010
http://www.irit.fr/SD4RCES/

==========

- Important dates:

* Paper submission: August 13, 2010
* Acceptance Notification: August 25, 2010
* Camera Ready version: September 1, 2010
* Workshop day: September 14, 2010

- Publication:

Accepted papers will be published in the ACM Digital Library in the ICPS series with the ISBN number 978-1-4503-0368-2

-CFP:

The main focus of SD4RCES is on the topic of making security and dependability expert knowledge available to Resource Constrained Embedded Systems (RCES) engineering processes. Special emphasis will be devoted to promote discussion and interaction between researchers and practitioners focused on the particularly challenging task to efficiently integrate security and dependability solutions within the restricted available design space for RCES. Furthermore, one important focus is on the potential benefits of the combination of model-driven engineering with pattern-based representation of security and dependability solutions. The workshop aims to bring together researchers from various fields involved in the development and deployment of RCES with a particular focus on the transfer of results from fundamental research to the industrial development of RCES. We believe that the synergy between researchers working in different aspects of this area will produce important benefits. The objective of this workshop is to foster an exchange of ideas among practitioners, researchers and industry involved in the deployment of secure and dependable resource-constrained embedded systems. The exchange of concepts, prototypes, research ideas, and other results which contribute to the academic arena and also benefit business and industrial communities, is of particular interest. Some of the topics that we seek to include in the workshop are related to the development of models and tools to support the inclusion of security and dependability (S&D) issues into the RCES engineering process. Topics of interest include, but are not limited to:

- Verification, testing and validation of S&D by design in RCES
- Design process of S&D patterns
- Model-based repository of S&D patterns for RCES
- Formalization of S&D properties at the pattern level
- S&D requirements engineering for RCES
- Inheritance of S&D properties upon integration of patterns
- Integration process of S&D patterns
- Customization of application sector specific processes
- Support tools for assisting modeling, deployment and configuration of S&D by design
- RCES development and engineering processes
- Case studies, empirical results, experience reports, etc...

- Submission:

We are inviting the submission of papers with high quality research contributions, work in progress, experimental and ongoing projects results. The following types of submission are accepted:

* Long papers (10 pages): reporting substantial, completed, and previously unpublished research.
* Short papers (6 pages): describing work in progress or industrial experiences,

* Format: All submitted papers must be written in English and conform to the ACM double column format (10pt, single-space, double-column and include an abstract of up to 150 words...). The format of the submission should follow ACM Formatting Guidelines (http://www.acm.org/sigs/publications/proceedings-templates). The submission should be done in PDF-format via our submission system before August 13, 2010.

- Co-organizers :

* Brahim Hamid (IRIT-University of Toulouse , France), brahim.hamid@irit.fr
* Carsten RUDOLPH (Fraunhofer Institute for Secure Information Technology SIT), carsten.rudolph@sit.fraunhofer.de
* Christoph RULAND (University of Siegen), christoph.ruland@uni-siegen.de

- Program Committee:

* Yemine Ait Ameur (LISI/ENSMA-UP, Univ. Poitiers)
* Jean-Michel Bruel (IRIT, Univ. Toulouse)
* Mireille Blay-Fornarino(I3S, Univ. Nice)
* Pierre Castéran (LABRI, Univ. Bordeaux)
* Nora Cuppens (ENST Bretagne)
* Khalil Drira (LAAS-CNRS)
* Amnon Eden (Foundations and Applications Research Group, Univ. Essex)
* Mamoun Filali (IRIT, Univ. Toulouse)
* Andreas Fuchs (Fraunhofer SIT)
* Sigrid Gürgens (Fraunhofer SIT)
* Christophe Gransart (INRETS)
* Cyril Grepet (Trialog)
* Brahim Hamid (IRIT, Univ. Toulouse)
* Erno Jeges (SEARCH lab, Hungary)
* Christophe Jouvray (Trialog)
* Oliver Jung (Research Center for Telecommunications, Vienna)
* Antonio Mana (Univ. Malaga)
* Fabio Massacci (Univ. Trento)
* Mohamed Mosbah (LABRI, Univ. Bordeaux)
* Simin Nadjm-Tehrani (Real-time systems lab, Univ. Linköping)
* Jan Pelzl (Escrypt)
* Christian Percebois (IRIT, Univ. Toulouse)
* Antonio Perez (Ikerlan-K4)
* Ansgar Radermacher (CEA List)
* Carsten Rudolph (Fraunhofer SIT)
* Christoph Ruland (Univ. Siegen)
* Maurizio Palesi (Univ. Catania)
* Francesca Saglietti (Univ. Erlangen-Nurnberg)
* Lionel Seinturier (LIFL-INRIA ADAM, Univ. Lille)
* François Terrier (CEA LIST)
* Salvador Trujillo (Ikerlan-K4)
* Didier Van-Den-Abeele (Transport/ALSTOM)
* Tulio Vardanega (Univ. Padou)
* François Vernada (LAAS-CNRS)