DSD2011

14th EUROMICRO CONFERENCE on DIGITAL SYSTEM DESIGN
Architectures, Methods and Tools

August 31- September 2, 2011 Oulu, Finland

Call for Papers

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Scope

The Euromicro Conference on Digital System Design (DSD) addresses all aspects of (embedded, pervasive and high-performance) digital and mixed hardware/software system engineering, down to microarchitectures, digital circuits and VLSI techniques. It is a discussion forum for researchers and engineers from academia and industry working on state-of-the-art investigations, development and applications. It focuses on advanced circuit and system design and design automation concepts, paradigms, methods and tools, as well as on modern implementation technologies from full custom in nanometer technology nodes to FPGA and to multicore infrastructures. Compiler assisted ASIP, CMP, SMP, SMT, DSP-VLIW, GPU and platform based system design research results are welcome. Design and Verification Languages and Standards, High Level Synthesis, Efficiency, Density, Signal Integrity, Testability, Timing Analysis and Timing Closure, Asynchronous Techniques, Reconfigurable Architectures, Power Consumption, Computational Power Speed and Performance, Productive Design Technology and Engineering Flows, Manufacturability, Cost, Reliability, Error Resilience, Complexity, Modeling, Design Experiences are covered in DSD.

Main Topics

T1: (SHES) System, hardware and embedded software design and automatic synthesis: high-level, behavioral, register-transfer, logic and physical circuit synthesis; arithmetic, signal processing and vector processing units; graphics processing units and hardware accelerators; memory design; communication architecture and protocols; specific circuits and processors; multi-objective optimization observing power, performance, communication traffic, interconnect architecture, layout, technology, reliability, robustness, security, testability and other issues; management of parallel computational resources, memory allocation and hierarchy; hardware/software co-design; mapping of applications to architectures; algorithm architecture matching; transaction level modeling and higher-level modeling; virtual system prototyping; design space exploration; synthesis of asynchronous and dataflow driven systems, nanoelectronics; CAD for placement, routing, retiming, logic optimization, technology mapping, system-level partitioning, logic generators, testing and verification; CAD for modeling, analysis and optimization of timing and power.

T2: (SoC & NoC) Systems-on-a-chip and networks-on-a-chip: multiprocessor systems on-a-chip (MPSoC), generic system platforms and platform-based design; CMP, SMP, SMT, DSP, VLIW and ASIP (multi)processor architectures and enhancements; 3D MPSoCs; software design and programming models for multicore platforms; benchmarks; GPUs; cell-based platforms; NoC architectural issues, quality of service in NoCs; 3D NoCs; power dissipation and energy issues in SoCs and NoCs; IP design, standardization and reuse; parallelism and scalability techniques; virtual components; system on a system; compiler assisted MPSoC; hardware support for embedded kernels; embedded software features; static, run-time and dynamic optimizations of embedded systems.

T3: (RC) Programmable/re-configurable/adaptable architectures: design methodologies and tools for reconfigurable computing, run-time, partial and dynamic reconfigurability; fine-grained, mixed-grained and coarse-grained reconfigurable architectures; reconfigurable interconnections and NoCs; FPGAs; systems on re-configurable chip; system FPGAs and structured ASICs and co-processors; processing arrays; programmable fabrics; novel logic block architectures, combination of FPGA fabric and system blocks (DSP, processors, memories, etc.); adaptive computing devices, systems and software; adaptable ASIPs and ASIP-based SOCs, hardware accelerators; optimization of FPGA-based cores; shared resource management; novel design algorithms for FPGA features; high-level models and tools for FPGAs; rapid prototyping systems and platforms; wireless and mobile systems.

T4: (SMVT) System, hardware and embedded-software specification, modeling, verification and test: design, modeling, simulation and verification languages; functional, structural and parametric specification and modeling, model-based design and verification; system, hardware, and embedded software analysis; simulation, emulation, prototyping, formal verification, design-for-test and testing at all design levels; dependability and fault-tolerance issues.

T5: (APP) Applications of (embedded) digital systems: emphasis on design challenges posed by demanding and new applications in fields such as: (wireless) communication and networking; networked electronic media, multimedia and ambient intelligence; image and video processing; mobile systems; health-care and medicine; ubiquitous, wearable and implanted systems; military, space, avionics, measurement, control and automotive applications; wireless sensor network applications; surveillance and security; environmental, agriculture, urban, building, transportation, traffic, energy, hazards and disasters monitoring and control.

T6: (ET) Important issues introduced by emerging technologies: issues for the system, circuit and embedded software design introduced by e.g. the nanometer CMOS and beyond CMOS technologies, 3D integration, optical and new memory technologies etc.; new human-machine interfaces, neural- and bio-computation, (bio)sensor and sensor network technologies, pervasive and ubiquitous computing, "internet of things"; design methods and EDA tools for solving these issues.

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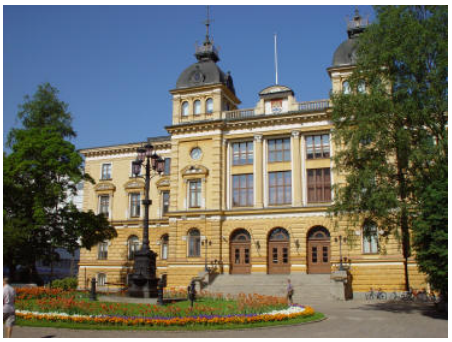

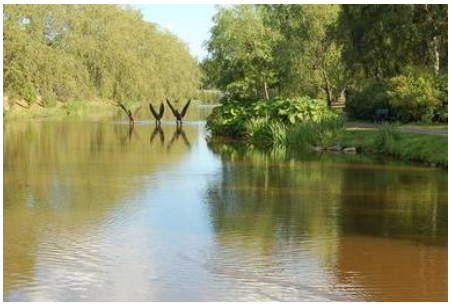

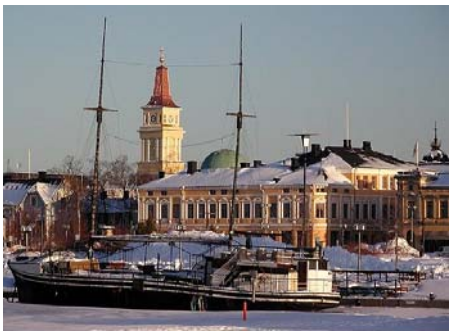

Special Sessions

SS1: (FDR) Flexible Digital Radio. HW / SW partitioning for flexible radios, HW accelerators for flexible radios, Algorithm / Architecture optimization, HW factorization and parameterization techniques, Design space exploration methodology, Parallel processing for real-time digital communication systems, Power consumption aware radios, Abstraction layers for multi-standard radio, Open platforms for multi-standard support, Prototypes, Application of flexible radio to cognitive radio.

SS2: (MSDA) Multicore Systems: Design and Applications. A forum for engineers and scientist to address challenges, and present new ideas in the multicore field, as well as introduce emerging implementations, and tackle related issues with respect to improving system performance and reducing energy consumption for multicore systems, as a whole.

SS3: (DTDS) Dependability and Testing of Digital Systems. Built-in self-Test, Off-line BIST and on-line BIST, SoC and NoC testing, Test compression methods, Error detection and correction, Testability analysis, Scan-based techniques, IDDQ and current testing Synthesis for testability, Diagnosis & testing of embedded systems, Analog, Mixed-Signal and RF, Testing memory and processor testing, System diagnosis.

SS4: (FTDSD) Fault Tolerance in Digital System Design. Fault tolerant design, FPGA based fault tolerant systems, SEU / SET effects, Concurrent error detection, Duplex/TMR/NMR systems, Partial / Full reconfiguration, Reliability parameters of fault tolerant systems and their evaluation.

SS5: (SLEO) System-Level Energy Optimization of HW/SW Embedded Systems. Optimization of the energy at different abstraction levels: from the design of code up to the library and task/resource management carried out at the system level.

SS6: (WSN) Wireless Sensor Networks. Architectures, Operating systems, Communication protocols, Protocol stacks, Design methods, EDA tools, Programming models, Computational modeling (timing, energy), Performance analysis and optimization, Simulation, Adaptivity, Self-organization, Control, Multi-modal sensing, Sensor fusion, Information processing, Mesh networking, Body-area networking, Applications in transport and mobility, Agriculture, Environmental and urban monitoring, Healthcare and elderly care, Home automation and assisted living, Prototypes, Field tests, Node designs, Tradeoffs between computation and communication, Analog vs. digital.

SS7: (AHSA) Architectures and Hardware for Security Applications. Efficient hardware architectures for public-key and secret-key cryptographic algorithms, Processors and co-processors for cryptography applications, Smart card crypto-processors, True and pseudorandom number generators, Reconfigurable hardware for cryptography, FPGA design security, Security architectures for pervasive computing and wireless applications, All types of attacks against implementations, Hardware trojans and trusted ICs.

SS8: (M2APS) - Monitoring Methods for Adaptive Parallel Systems. Adaptive parallel systems need to be able to reconfigure themselves dynamically by monitoring their own condition and the surrounding environment and adapt themselves to different scenarios and requirements. Runtime monitoring becomes crucial in the emerging and future parallel systems due to increase in variations and fault occurrences. Furthermore, to obtain optimal performance-power ratio, for both single-chip and physically distributed parallel systems, monitoring is essential to have system wide adaptability.

Submission Guidelines

Regular Papers: Prospective authors are encouraged to submit their manuscripts for review electronically through the following web page (https://www.conftool.net/dsd2011/) or by sending the paper to the Program Chair via email (pkitsos@eap.gr, only if an unexpected web access problem is encountered) before the deadline for submission.

Each manuscript should include the complete paper text, all illustrations, and references. The manuscript should conform to the required IEEE format: single-spaced, double column, A4/US letter page size, 10-point size Times Roman font, up to 8 pages. In order to conduct a blind review, no indication of the authors' names should appear in the submitted manuscript, references included.

Case Studies and Application Papers: Submissions can be made which report on state-of-the-art digital systems, digital designs, architectures, design methods and/or tools, and (embedded) applications. Papers discussing lessons learned from practical experience, demanding or new applications, and experimental research are particularly encouraged. Manuscripts may be submitted in the same way as regular papers.

Presentation of Papers: The Program Committee members will decide if papers will be accepted for a long presentation (30 minutes), short presentation (15 minutes) or as a poster. For long and short presentations, 8 pages will be assigned in the published proceedings. A poster presentation will be assigned 4 pages. Papers exceeding the page limit will be charged 50 Euro per page in excess. If the paper is accepted, at least one of the authors must pre-register and pay the conference fee before the deadline for submitting the camera-ready paper. Otherwise the paper will not be published in the proceedings.

Publication of Papers: The IEEE Conference Publishing Services (CPS), publishes the DSD Proceedings, which are available worldwide through the IEEE Xplore Digital Library. An extended version of the best papers will be published in a special issue of the ISI-indexed *"Microprocessors and Microsystems: Embedded Hardware Design"* journal, printed by Elsevier Ltd.

Contact Information

Program Chair: Dr. Paris Kitsos
School of Science & Technology
Hellenic Open University (HOU)
13-15 Tsamadou str., Patras,
GR-26222, Greece
Phone : +30 2610 367535
Fax : +30 2610 367520
e-mail: pkitsos@eap.gr

Important Dates

- Submission of papers: March 14th, 2011
- Notification of paper acceptance: April 24th, 2011
- Camera ready papers: May 29th, 2011

Web Links

- DSD'11 web page: *http://dsmc2.eap.gr/dsd11*
- Euromicro web page: *http://www.euromicro.org*